AMENDMENTS

In the Title:

Please replace the Title with the following rewritten Title:

--FOUR TERMINAL SEMICONDUCTOR DEVICE AND METHOD FOR DRIVING THE SAME--

In the Claims:

Please amend claims 1, 6, 10, 18, and 22 as follows:

1. (Amended) A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and [a gate terminal fabricated on a channel region, formed between said source region and drain region, which receives a first input signal through a gate insulating film], wherein:

each of said semiconductor elements is electrically separated from the others; and

said well in each of said semiconductor elements is provided with a substrate terminal which receives a second input signal through a contact hole formed therein at a region other than said source region and drain region.

6. (Amended) The semiconductor device of Claim 1, wherein:

[each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element];

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form the first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form the second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

10. (Amended) A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region;

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

18. (Amended) A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region;

[each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;]

a drain terminal of said N-type semiconductor element is supplied with a high potential and a drain terminal of said P-type semiconductor element is supplied with a low potential;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

source terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

22. (Amended) The semiconductor device of Claim 1, wherein:

[each of said semiconductor elements is composed of a P-type semiconductor element and an N-type semiconductor element;]

a high potential is supplied to a drain terminal of said N-type semiconductor element and a low potential is supplied to a drain terminal of said P-type semiconductor element;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form the first input terminal;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form the second input terminal; and

source terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

In the Abstract:

Please replace the Abstract on page 67 with the following rewritten Abstract:

In a semiconductor element (1) provided with a source region (3) and a drain region (4) both formed in a well (2), and a gate electrode (7) fabricated on a channel region (5), formed between these regions, through a gate insulting film (6), each element is electrically isolated by means of an SOI substrate and a field oxide film, for example, and a substrate terminal (TW) is pulled out from the channel region (5) via a contact hole formed through an inter-layer insulating film in each element at a region other than the source region (3) and drain region (4). Consequently, a 2-input-1-output element having the gate terminal (TG) and substrate terminal (TW) as two inputs can be realized, thereby making it possible to improve a packing density and operating rate while reducing the costs when forming a logic circuit or the like.